

REMARKS

The Office rejected claims 1 and 2. With this paper, claims 1 and 2 are amended, none are canceled, and none are added.

Claim Rejections under 35 USC §102

Claim 1 is rejected under 35 USC 102(b) as being anticipated by Applicant's Admitted Prior Art (AAPA) (Figs. 3 and 4).

As shown in Figs. 3 and 4, an external output video signal processor known in the prior art comprises a system controller 10a and a video signal processing circuit unit 20a coupled with the system controller 10a via a capacitor 30. The prior art external output video signal processor is characterized in that the system controller 10a comprises a DSP unit 11, a resistance 12 and an impedance conversion circuit 13, and the video signal processing circuit comprises a clamp circuit 23 and a latter-part procession circuit 22.

The Applicant respectfully submits that the present invention is different from the prior art. In the present invention as shown in Figs. 1 and 2, the external output video signal processor comprises a system controller 10 and a video signal processing circuit 20. The system controller 10 and the video signal processing circuit 20 are directly coupled with each other without a capacitor between the two. The system controller 10 has a DSP unit for outputting a current signal and a resistance 12 for converting the current signal to a voltage signal. Since the output of the system controller 10 is directly coupled to the video signal processing circuit 20, there is no need for an impedance conversion circuit like the one in Fig. 3.

With this paper, Claim 1 is amended to clarify the above difference. Accordingly, the invention in claim 1 of the present invention is not the same as the arrangement of the circuit described in Figs. 3 and 4.

Based on the foregoing, it is believed that claim 1 is patentable. Applicant respectfully requests the rejection of claim 1 be reconsidered and withdrawn.

Claim Rejections under 35 USC §103

Claim 2 is rejected under 35 USC §103(a) as being unpatentable over AAPA.

As mentioned above, the present invention does not have a capacitor between the system controller 10 and the video signal processing circuit 20. As a result, a level shift circuit 21 having two stages of inverting amplifiers 213 and 217 is used in place of a clamp circuit 23. In the instant specification, the clamp circuit 23 is referred to as being disclosed, for example, in Japanese Unexamined Patent Publication No. 46443/1995. The clamp circuit as shown in the figure of 46443/1995 is structurally and functionally different from the level shift circuit 21 whose circuit diagram is shown in Fig. 2 of the instant application.

Therefore, the present invention as recited in claim 2 is not the same as the arrangement of the circuit described in Figs. 3 and 4. Compared to the arrangement in the prior art, the present invention reduces costs and space of the external output video signal processor. Moreover, the present invention helps to prevent shrinkage of a synchronizing signal and occurrence of sag in the signal. Claim 2 depends on claim 1 and claim 1 is believed to be patentable. Therefore claim 2 is patentable. Applicant respectfully requests the rejection of claim 2 be reconsidered and withdrawn.

Amendment in Drawings

A replacement sheet containing Figs. 1 and 2 is submitted with this paper. A change is made in Fig. 1 to replace the label of numeral 21 with the label "LEVEL SHIFT CIRCUIT." "Level shift circuit" is used throughout the specification. Entry of the amended Fig. 1 is respectfully requested.

Conclusion

For all the foregoing reasons, it is believed that all the claims of the instant application are patentable, and their passage to issue is earnestly solicited. Applicant's agent urges the Examiner to call to discuss the present response if anything in the present response is unclear or unpersuasive.

Respectfully submitted,



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